The following listing of claims will replace all prior versions, and listings, of claims in the present application.

LISTING OF THE CLAIMS:

Claims 1- 13 (Cancelled)

Claim 14 (Currently Amended) A low-resistance T-gate MOSFET comprising:

a Si-containing substrate comprising at least one device channel/body implant region separating a source region from a drain region, said at least one device channel/body implant region having a length of less than about 0.1 μm;

a gate dielectric located at least atop said device channel/body implant region, said source region and said drain region;

a T-gate located atop a portion of said gate dielectric, said T-gate comprises a recessed bottom polysilicon region and an upper gate conductor region, said upper gate conductor region has a width that is greater than a width of said bottom polysilicon region and comprises a lower polysilicon portion and an upper portion including one of Al, W, Cu, Ti and a silicide ~~is selected from the group consisting of polysilicon, Al, W, Ti, a silicide and any combination thereof~~; and

nitride spacers located on exposed vertical sidewalls of said bottom polysilicon region, said nitride spacers have an outer edge that is aligned with an outer edge of the upper gate conductor region.

Claim 15 (Original) The low-resistance T-gate MOSFET of Claim 14 wherein said gate dielectric is an oxide having a dielectric constant of about 3.0 or greater.

Claim 16 (Original) The low-resistance T-gate MOSFET of Claim 14 wherein said Si-containing substrate is a component of a silicon-on-insulator wafer.

Claim 17 (Cancelled)

Claim 18 (Currently Amended) The low-resistance T-gate MOSFET of Claim 17 wherein said upper portion of said gate conductor is composed of Al, W, or Ti.

Claim 19 (Currently Amended) The low-resistance T-gate MOSFET of Claim 14 wherein said upper portion of said gate conductor is composed of W.

Claim 20 (Cancelled)

Claim 21 (Currently Amended) A low-resistance T-gate MOSFET comprising:

a Si-containing substrate comprising at least one device channel/body implant region separating a source region from a drain region, said at least one device channel/body implant region having a length of less than about 0.1 μm;

a gate dielectric located at least atop said device channel/body implant region, said source region and said drain region;

a T-gate located atop a portion of said gate dielectric, said T-gate comprises a recessed bottom polysilicon region and an upper gate conductor region comprising an upper portion of W located on a lower portion of polysilicon, said upper gate conductor region has a width that is greater than a width of said bottom polysilicon region; and

nitride spacers located on exposed vertical sidewalls of said bottom polysilicon region, said nitride spacers have an outer edge that is aligned with an outer edge of the upper gate conductor region.

Claim 22 (Cancelled)